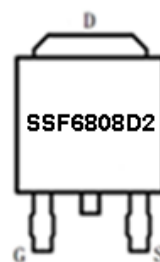


**Main Product Characteristics:**

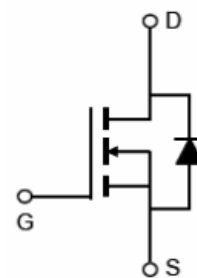
$V_{DSS}$	60V
$R_{DS(on)}$	7m $\Omega$ (typ.)
$I_D$	80A



TO-252 (DPAK)



Marking and pin Assignment



Schematic diagram

**Features and Benefits:**

- Advanced MOSFET process technology
- Special designed for PWM, load switching and general purpose applications
- Ultra low on-resistance with low gate charge
- Fast switching and reverse body recovery
- 175°C operating temperature


**Description:**

It utilizes the latest processing techniques to achieve the high cell density and reduces the on-resistance with high repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in power switching application and a wide variety of other applications.

**Absolute max Rating:**

Symbol	Parameter	Max.	Units
$I_D$ @ TC = 25°C	Continuous Drain Current, $V_{GS}$ @ 10V ①	80	A
$I_{DM}$	Pulsed Drain Current ②	180	
$P_D$ @TC = 25°C	Power Dissipation ③	110	W
$V_{DS}$	Drain-Source Voltage	60	V
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$E_{AS}$	Single Pulse Avalanche Energy @ L=0.5mH	390	mJ
$T_J$ $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to +175	°C

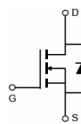
## Thermal Resistance

Symbol	Characterizes	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-case ③	—	1.36	$^{\circ}\text{C}/\text{W}$

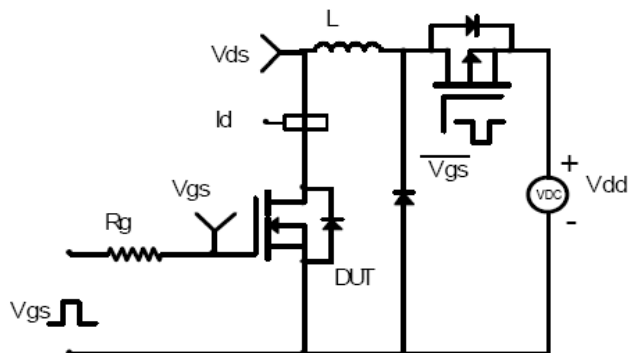
## Electrical Characterizes @ $T_A=25^{\circ}\text{C}$ unless otherwise specified

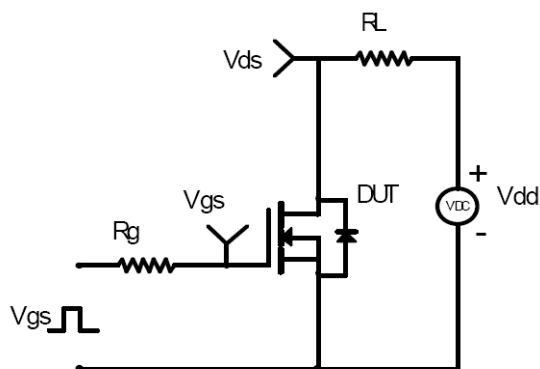
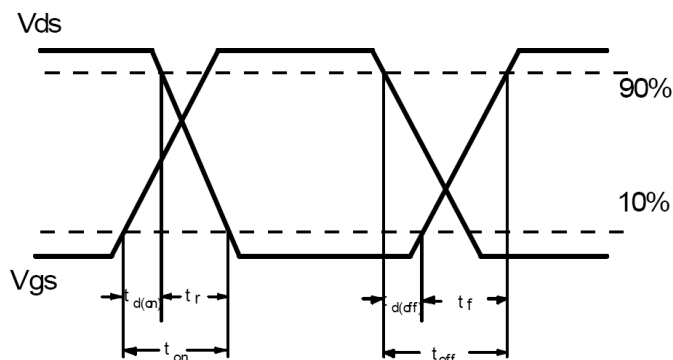
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source breakdown voltage	60	—	—	V	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$
$R_{DS(on)}$	Static Drain-to-Source on-resistance	—	7	8.5	$\text{m}\Omega$	$V_{GS}=10\text{V}, I_D=20\text{A}$
$V_{GS(th)}$	Gate threshold voltage	2	2.8	4	V	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$
$I_{DSS}$	Drain-to-Source leakage current	—	—	1	$\mu\text{A}$	$V_{DS} = 60\text{V}, V_{GS} = 0\text{V}$
$I_{GSS}$	Gate-to-Source forward leakage	—	—	100	nA	$V_{GS} = 20\text{V}$
		—	—	-100		$V_{GS} = -20\text{V}$
$Q_g$	Total gate charge	—	90	—	nC	$I_D = 10\text{A},$ $V_{DS}=75\text{V},$ $V_{GS} = 10\text{V}$
$Q_{gs}$	Gate-to-Source charge	—	9	—		
$Q_{gd}$	Gate-to-Drain("Miller") charge	—	18	—		
$t_{d(on)}$	Turn-on delay time	—	8.5	—	ns	$V_{GS}=10\text{V}, V_{DS}=30\text{V},$ $R_{GEN}=3\Omega$ $R_L=1\Omega$
$t_r$	Rise time	—	7	—		
$t_{d(off)}$	Turn-Off delay time	—	40	—		
$t_f$	Fall time	—	15	—		
$C_{iss}$	Input capacitance	—	4000	—	pF	$V_{GS} = 0\text{V}$
$C_{oss}$	Output capacitance	—	290	—		$V_{DS} = 30\text{V}$
$C_{rss}$	Reverse transfer capacitance	—	210	—		$f = 1\text{MHz}$

## Source-Drain Ratings and Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	80	A	MOSFET symbol showing the integral reverse p-n junction diode. 
$V_{SD}$	Diode Forward Voltage	—	—	1.2	V	$I_S=20\text{A}, V_{GS}=0\text{V}$
$t_{rr}$	Reverse Recovery Time	—	32	—	ns	$I_S=20\text{A}, di/dt=100\text{A}/\mu\text{s}$
$Q_{rr}$	Reverse Recovery Charge	—	45	—	nC	

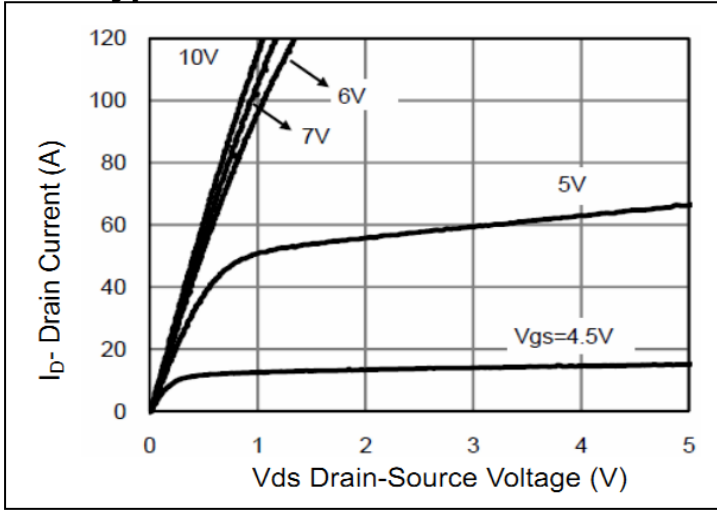
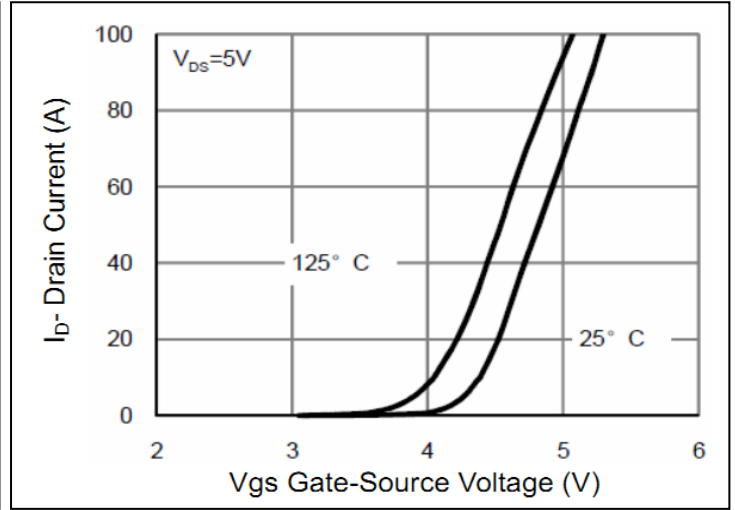
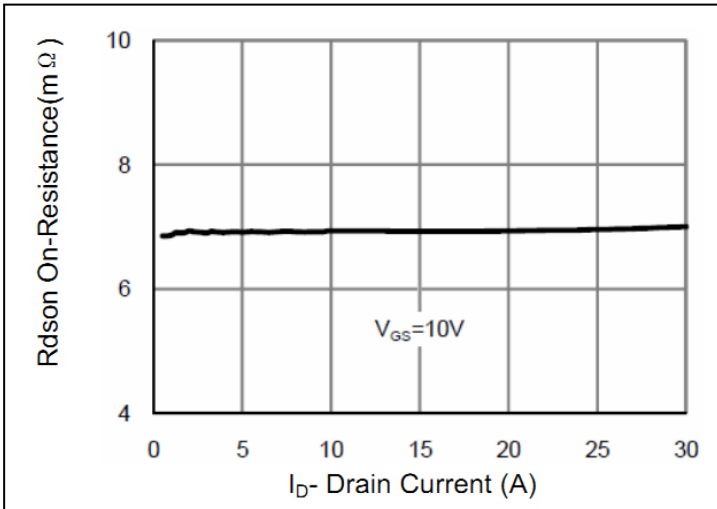
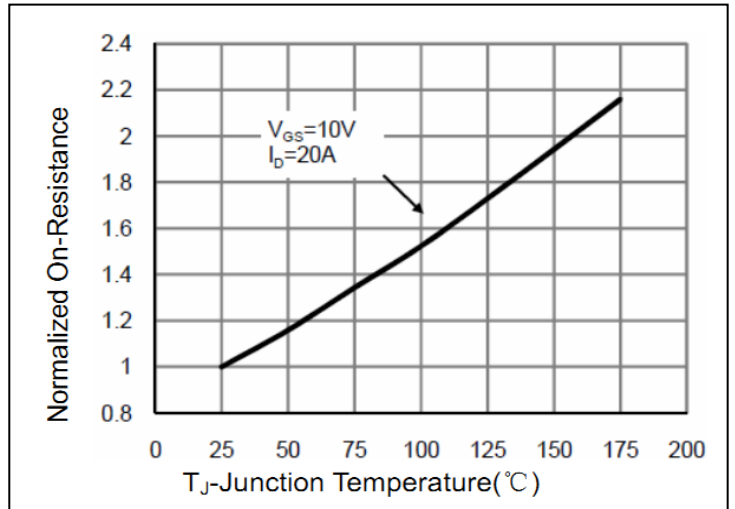
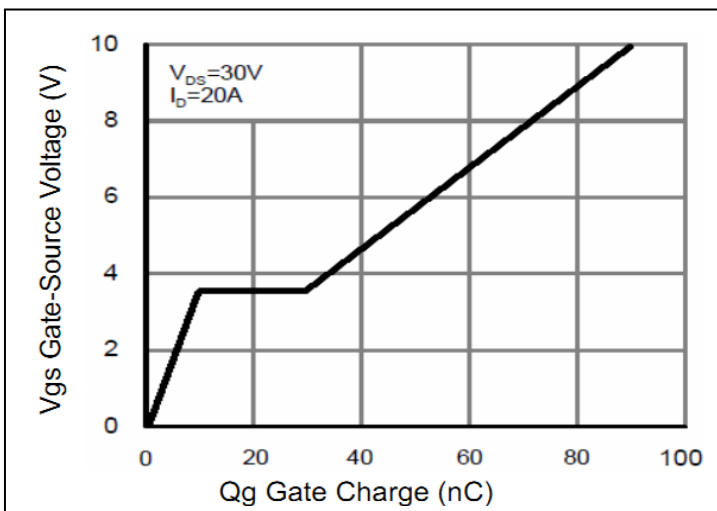
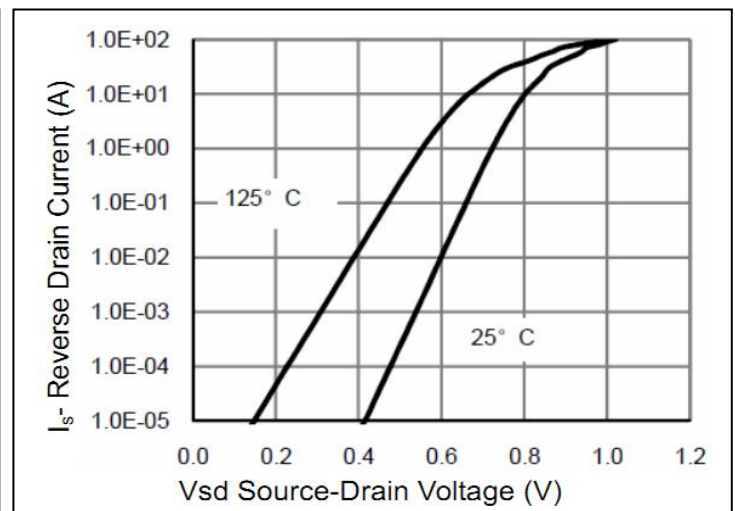
## Test circuits and Waveforms

**EAS Test Circuit:**

**Gate charge test circuit:**

**Switching Time Test Circuit:**

**Switching Waveforms:**


### Notes:

- ① Calculated continuous current based on maximum allowable junction temperature.
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ The power dissipation PD is based on max. junction temperature, using junction-to-case thermal resistance.

**Typical electrical and thermal characteristics**

**Figure 1: Typical Output Characteristics**

**Figure 2: Transfer Characteristics**

**Figure 3: Rdson-Drain Current**

**Figure 4: Rdson-Junction Temperature**

**Figure 5: Gate Charge**

**Figure 6: Source-Drain Diode Forward**

Typical electrical and thermal characteristics

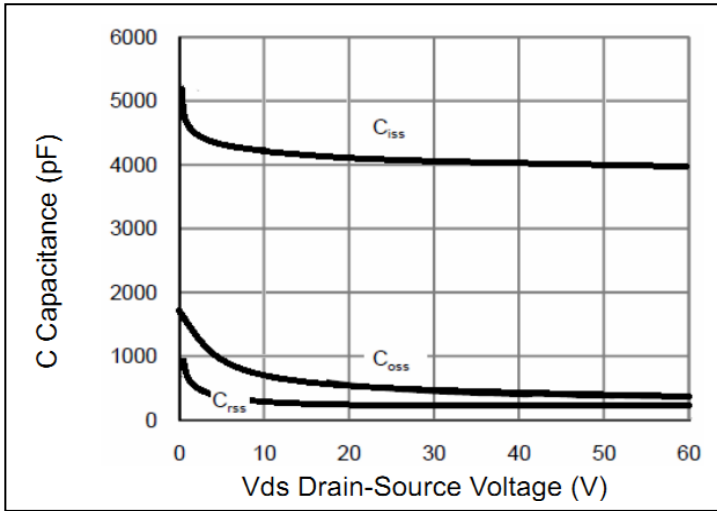


Figure 7: Capacitance vs Vds

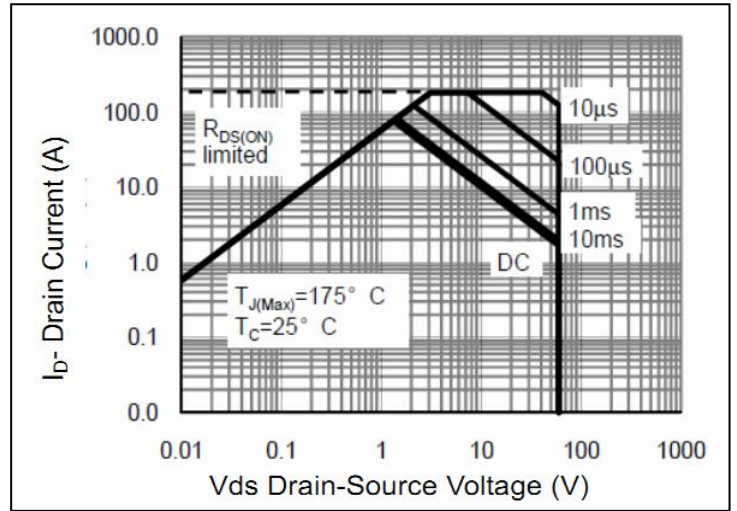


Figure 8: Safe Operation Area

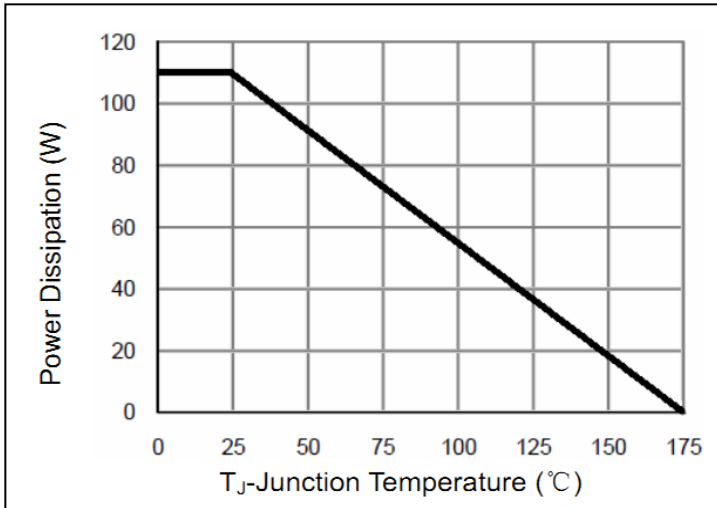


Figure 9: Power De-rating

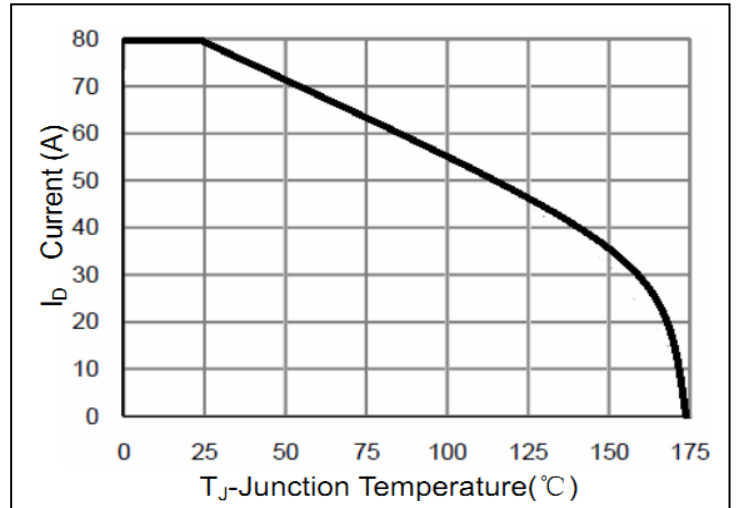


Figure 10: ID Current-Junction Temperature

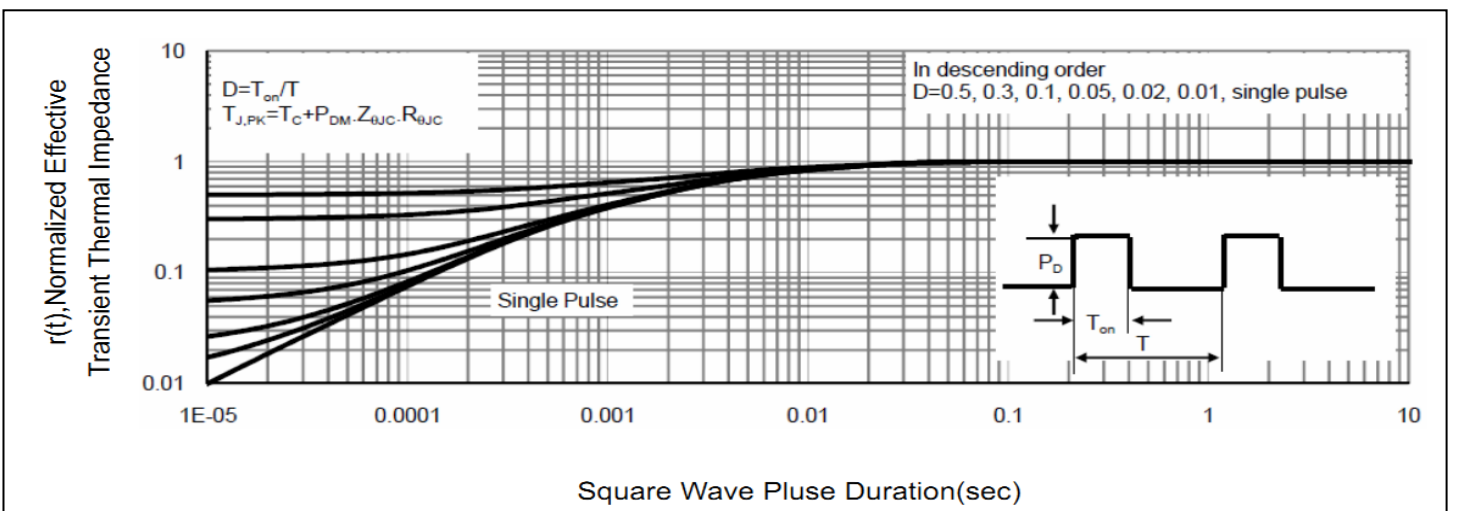
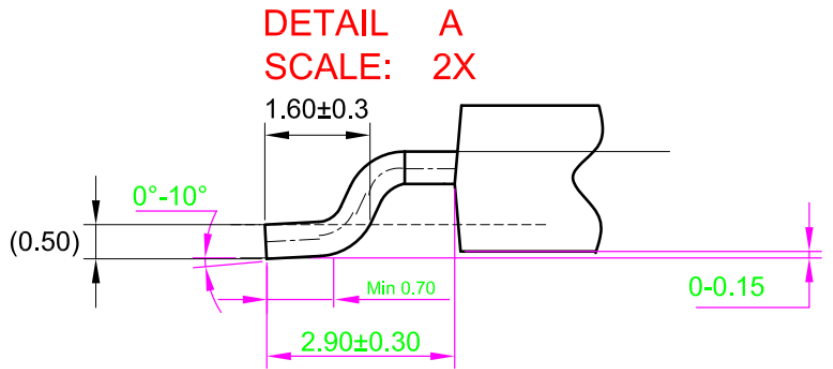
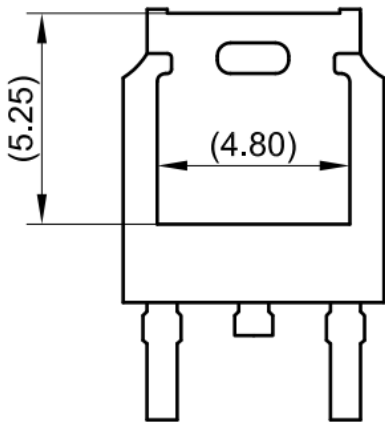
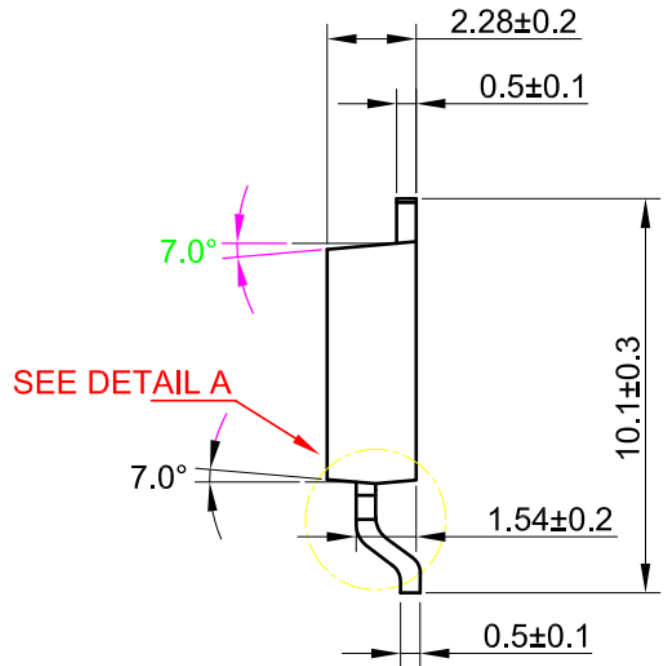
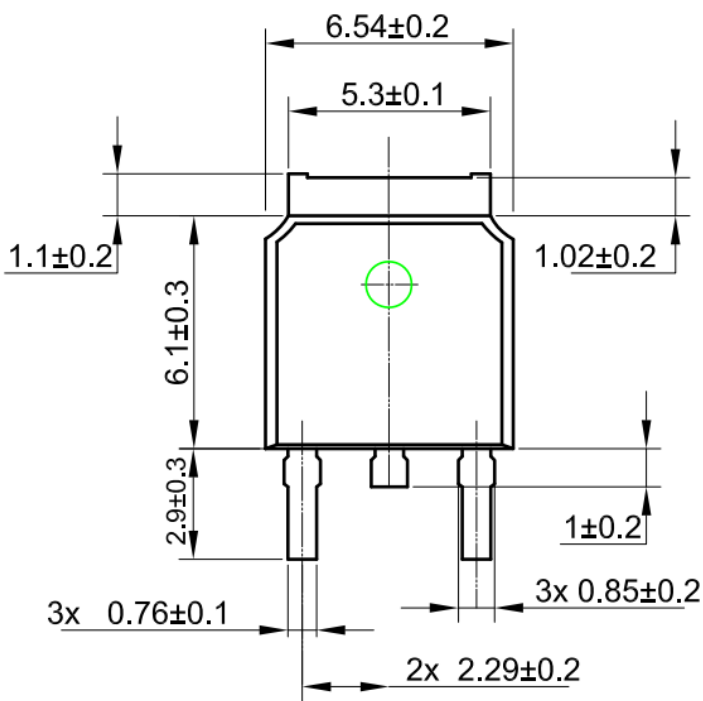


Figure 11: Normalized Maximum Transient Thermal Impedance

Mechanical Data:



**Ordering and Marking Information**
**Device Marking: SSF6808D2**

**Package (Available)**  
**TO-252(DPAK)**  
**Operating Temperature Range**  
**C : -55 to 175 °C**

**Devices per Unit**

Package Type	Units/Tape	Tapes/Inner Box	Units/Inner Box	Inner Boxes/Carton Box	Units/Carton Box
TO-252	2500	2	5000	7	35000
TO-252	2500	1	2500	10	25000
TO-252	800	5	4000	8	32000

**Reliability Test Program**

Test Item	Conditions	Duration	Sample Size
High Temperature Reverse Bias(HTRB)	$T_j=125^{\circ}\text{C}$ to $150^{\circ}\text{C}$ @ 80% of Max $V_{DSS}/V_{CES}/V_R$	168 hours 500 hours 1000 hours	3 lots x 77 devices
High Temperature Gate Bias(HTGB)	$T_j=150^{\circ}\text{C}$ @ 100% of Max $V_{GSS}$	168 hours 500 hours 1000 hours	3 lots x 77 devices

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